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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/468,051	12/20/1999	THOMAS D. HARTNETT	RA-5271	3159

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EXAMINER	
WOOD, WILLIAM H	

ART UNIT	PAPER NUMBER
2124	15

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Please find below and/or attached an Office communication concerning this application or proceeding.

PRE

Office Action Summary	Application No. 09/468,051	Applicant(s) HARTNETT ET AL.	
	Examiner William H. Wood	Art Unit 2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 21-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 21-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claims 1-7 and 21-46 are pending and have been examined.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 21, 27, 32, 39, 40 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Bhamidipati** et al. (USPN 6,112,295) in view of **Hayes**, John P., "Computer Architecture and Organization". Maintained as previously presented (not repeated for brevity).

3. Claims 2-6, 22-25, 28-30, 33-38, 41-43 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Bhamidipati** et al. (USPN 6,112,295) in view of **Hayes**, John P., "Computer Architecture and Organization" and in further view of **Kyker** et al. (USPN 6,026,477). Maintained as previously presented (not repeated for brevity).

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Bhamidipati** et al. (USPN 6,112,295) in view of **Hayes**, John P., "Computer Architecture and Organization" in view of **Kyker** et al. (USPN 6,026,477) and in further.

view of **Alferness** et al. (USPN 5,577,259). Maintained as previously presented (not repeated for brevity).

5. Claims 26, 31 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Bhamidipati** et al. (USPN 6,112,295) in view of **Hayes**, John P., "Computer Architecture and Organization" and in further view of **Alferness** et al. (USPN 5,577,259). Maintained as previously presented (not repeated for brevity).

Response to Arguments

6. As an initial matter, previously presented 35 U.S.C 112 rejections (paper 12, mailed 19 June 2003) concerning new matter are withdrawn.

7. Applicant's arguments filed 23 October 2003 with regard to the independent claims have been fully considered but they are not persuasive. Applicant argued: [i] **Bhamidipati**'s decoupling queue does not suggest independent movement of instructions in an execution circuit from a fetch circuit; [ii] placement of the queue between any stage could eliminate direct coupling of a fetch circuit and an execution circuit; [iii] **Hayes** in unnecessary; [iv] **Hayes** does not provide for asserted deficiencies of **Bhamidipati**; [v] one would not be motivated to combine **Hayes** and **Bhamidipati**; and [vi] use of impermissible hindsight. Applicant is incorrect on each issue.

As to the first issue, **Bhamidipati** states decoupling queues are used to allow for independence of the various circuits within a pipeline (column 1, lines 23-35). As to the second issue, **Bhamidipati** disclosed placement of the queue between many stages

(column 3, lines 53-57) even multiple queues between several stages (column 1, lines 23-35). Applicant makes an assumption that separating some stages from other stages breaks to requirement that the instructions within an execution circuit and a fetch circuit are independently advancing and the two circuits are *directly* coupled. However, the queue in one embodiment could be considered part of one of the circuits (fetch or execution). The terms stage and circuit are far too broad to limit the physical hardware making up the stages or circuits (a queue within a stage or circuit is still directly coupled to the next stage or circuit). Said terms are abstractions used by humans. As to the third issue, **Hayes** is necessary in so much as an example of how fetch circuits and execution circuits can be directly coupled (the rejection states **Bhamidipati** does not *explicitly* state ...). Applicant assumes A and X constitute an execution circuit though this may be the case it might just as well not be the case. This would depend on one of ordinary skill in the art's definition of an execution circuit, which depending on circumstances would be highly variable (for example; including floating point processing; order of various execution steps; and how inclusive is the term execution, is computing operand address "house keeping" or actual execution). It is noted, though, that Applicant would consider the A and X partitions all part of the execution circuit (this interpretation would strengthen the position that **Bhamidipati** is read upon). Additionally, Applicant is reminded of the above statements concerning the placement of the queues (within circuits). As to the fourth issue, Applicant is reminded that under a 35 U.S.C 103 rejection both references are taken together. **Hayes** was provided for the specific teaching of direct coupling as stated in the previously presented rejection.

Bhamidipati disclosed other necessary details of Applicant's claim. As to the fifth issue, Applicant is apparently trying to build something new out of **Bhamidipati** and **Hayes**. However, **Hayes** is more of an example of a configuration of **Bhamidipati**. One of ordinary skill in the art is motivated by the fact that such configuration exists as shown by **Hayes**. As to the sixth issue, in response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). Finally, Applicant is encouraged not to focus on a specific mapping of **Bhamidipati**'s and **Hayes**' stages and elements to form the fetch and execution circuits. The term stage and circuit are too fluid for such and interpretation. Furthermore, **Bhamidipati** disclosed a general concept of a decoupling queue, which under the current broadly written claims is read upon by Applicant. **Hayes** does not teach away from Applicant's claimed invention it illuminates **Bhamidipati**.

8. Applicant's arguments filed 23 October 2003 with regard to all other claims have been fully considered but they are not persuasive. Applicant argued: [i] **Kyker** does not teach entry of an instruction into a pre-decode or decode stage independently of the movement of instructions through an execution circuit; [ii] cited prior art does not disclose retrieving from a queue instructions for the fetch stages independent of the execution

stages; [iii] **Kyk r** does not teach or suggest allowing for retrieval of an instruction from either the memory or from the queue; [iv] cited prior art does not disclose pre-decode stages independent of extended mode execution stages processing non-advancing instructions; and [v] impermissible hindsight. Applicant is again incorrect on each issue.

As to the first issue, once again Applicant is reminded to consider all references together. **Kyker** demonstrates multiple decode stages and **Bhamidipati** and **Hayes** demonstrate decoupling fetch and execution circuits (decode being part of the fetch circuit). As to the second issue, **Bhamidipati** most definitely disclosed a queue. Furthermore, **Bhamidipati** disclosed the possibility of multiple queues at various locations throughout the pipeline (column 1, lines 23-35). Clearly a queue can decouple the fetch and execution circuits and another queue be placed in the fetch circuit for additional decoupling. As to the third issue, Applicant is not addressing the previously presented rejection concerning the pipeline flush concept. As such, the previous rejection stands and is consider clear to Applicant. As to the fourth issue, again Applicant is reminded to consider all references together. **Alferness** disclosed extended stage execution. As noted above other references disclose decoupling circuits to increase pipeline performance. As to the fifth issue, hindsight is discussed above and repeated here.

9. It is believed that the above arguments address all of Applicant's raised issues and concerns. The previously presented rejections along with the above arguments clarify how Applicant's *claimed* invention does not overcome the cited prior art.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William H. Wood whose telephone number is (703)305-3305. The examiner can normally be reached 7:30am - 5:00pm Monday thru Thursday and 7:30am - 4:00pm every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703)305-9662. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7239 for regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

William H. Wood
January 6, 2004

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
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